LISTING OF THE CLAIMS (1-20)

Claim 1 (currently amended): A semiconductor device having a N-gate/N-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

an N doped substrate;

a gate oxide layer disposed over the N doped substrate;

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a first isolation oxide and a second isolation oxide disposed over the N doped substrate and on opposing edges of the gate oxide layer;

an N+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

Claim 2 (original): The semiconductor device of Claim 1, wherein the gate is in a depletion mode simultaneously while the N doped substrate is in an accumulation mode.

Claim 3 (original): The semiconductor device of Claim 1, wherein the polysilicon gate depletion of the semiconductor device corresponds to capacitor-voltage characteristics of the N-gate/N-substrate capacitor.

Claim 4 (currently amended): A semiconductor device having a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

a P doped substrate;

a gate oxide layer disposed over the ~~N-type~~P doped substrate;

a first isolation oxide and a second isolation oxide disposed over the ~~N-type~~P doped substrate;

a[[n]] P+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

Claim 5 (original): The semiconductor device of Claim 4, wherein the gate is in a depletion mode simultaneously while the substrate is in an accumulation mode.

Claim 6 (original): The semiconductor device of Claim 4, wherein the polysilicon gate depletion of the semiconductor device

corresponds to capacitor-voltage characteristics of the P-gate/P-substrate capacitor.

Claim 7 (original): A semiconductor capacitor structure, comprising:

an N doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

an N+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor is used to characterize polysilicon gate depletion corresponding to a semiconductor fabrication process.

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Claim 8 (original): The semiconductor capacitor of Claim 7, wherein the gate is in a depletion mode while the substrate is an accumulation mode.

Claim 9 (original): The semiconductor structure of Claim 7, wherein the polysilicon gate depletion corresponding to the semiconductor fabrication process is characterized by capacitor-voltage characteristics of the semiconductor capacitor.

Claim 10 (currently amended): A semiconductor capacitor structure, comprising:

an P doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

~~an N+ doped~~ a P+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor structure is used to characterize polysilicon gate depletion corresponding to a semiconductor process.

Claim 11 (original): The semiconductor device of Claim 10, wherein the gate is driven into depletion while the substrate is simultaneously driven into accumulation.

Claim 12 (original): The semiconductor device of Claim 10, wherein capacitance-voltage measurements are taken to characterize the polysilicon gate depletion of the semiconductor device.

Claims 13-20 (canceled)

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